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# ASSIGNMENT-2



## BASICS OF ELECTRONICS & COMM. ENGG.

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SECTION : C-72
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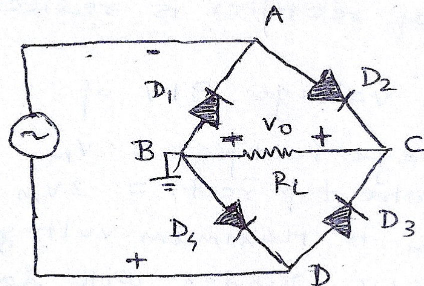
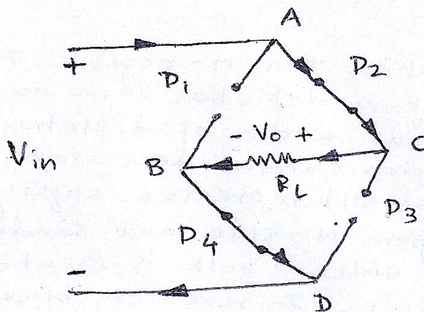
Q1.




Bridge rectifier circuit

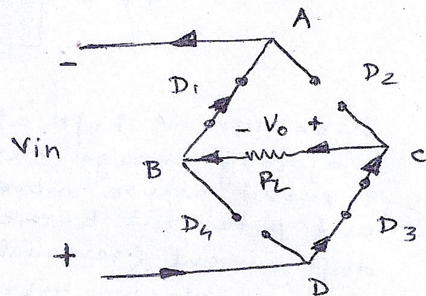
Considering diodes $D_1, D_2, D_3, D_4$ to be ideal.
∴ Act as open branches when reverse biased.
" short branches when forward biased.

CASE 1




$V_A > V_D$
∴ $D_2, D_4$ Forward Biased
& $D_1, D_3$ Reversed Biased.
∴ current Adops path ACBD

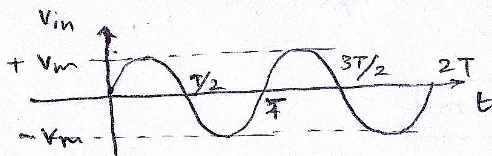
CASE 2



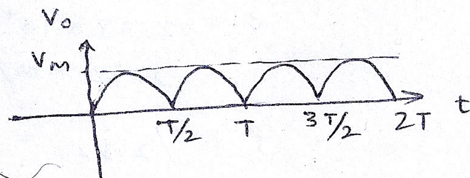

$V_D > V_A$
∴ $D_2, D_4$ reversed Biasd.
& $D_1, D_3$ forward Biased
∴ current Adops path DCBA.

∴ During both sycles of Alternating input signal. Current across load is established in same direcn : unidirectional pulsating current is obtained.

∴ INPUT

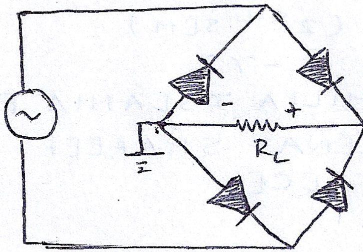



OUTPUT

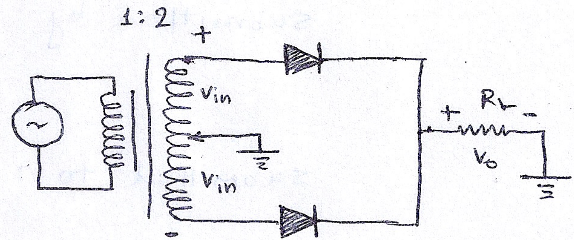


Advantages of Bridge rectifier over full wave rectifier

Bridge rectifier




Centre Tap rectifier




(1) In Bridge rectifier, need of transformer is removed. Hence size of rectifier is reduced.

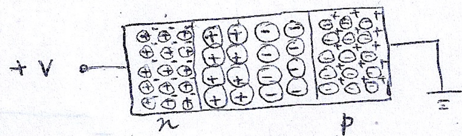
(2) Peak inverse voltage PIV of

Bridge rectifier = $V_m$.
centre tap rect. = $2V_m$

where $V_m$ is Maximum voltage input

Due to less PIV, Diodes with lower breakdown voltages can be used.

Q2 (a) working of diode in reverse bias.




P region is kept at lower potential than n-region. This forces majority charge carriers away from depletion layer and as a result expose more ions and thus width of depletion layer ↑ and potential barrier also. Diffusion current decreases while drift current (remaining negligibly small) increases slightly. For each electron taken by battery from N-side and sending it for recombination with holes on P side, a hole is created on N side which drifts back to P-side. In reversed bias state diode acts as an open switch if ideal until its breakdown at higher reverse voltages. In practical diode however a reverse saturation current flows due to increased drift current.

(b) for intrinsic semiconductor, conductivity is given as ~~(By Mass action law)~~

$$\sigma = nq(\mu_e + \mu_h)$$

where, $n$ : density of charge carriers
$q$ : charge of charge carriers
$\mu_e$ : mobility of electrons
$\mu_h$ : " " holes.

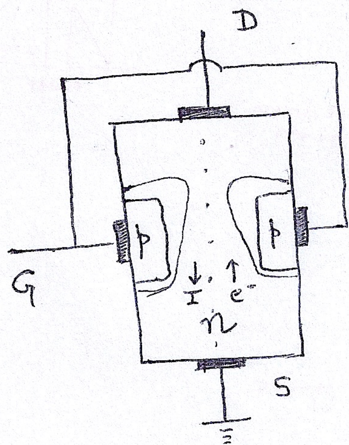
given, $n = 2.37 \times 10^{19}\ m^{-3}$
$\mu_e = 0.38\ m^2 v^{-1} s^{-1}$
$\mu_h = 0.18\ m^2 v^{-1} s^{-1}$

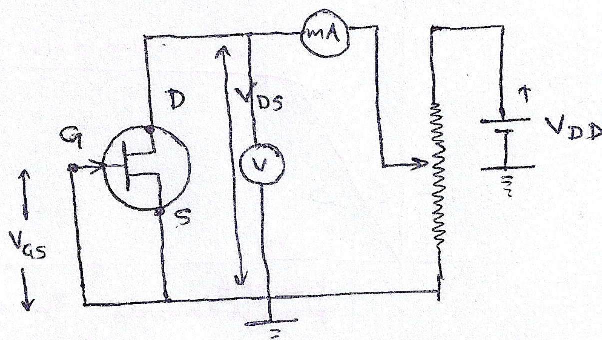
$$\sigma = 2.37 \times 10^{+19}\ m^{-3} \times 1.6 \times 10^{-19}\ As\,(0.38 + 0.18\ m^2 v^{-1} s^{-1})$$

$$= 2.12\ A/Vm$$

$$\rho = 1/2.12 = \boxed{0.471\ \Omega m}$$

Q 3 .




Circuit for determining I/O characteristics

Drain characteristics with shorted gate ($V_{GS} = 0$)

CASE 1 $V_{DS} = 0$

There is No Attracting potⁿ at drain → no current flows inspite channel is fully open.

$\therefore \quad I_D = 0$

CASE 2 $V_{DS} < V_{Pinch}$ → uptil knee pt $I_D \propto V_{DS}$.

knee pt to pinch off $I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$ (~~$V_{GS(off)}$~~)

As $V_{DS}$ is increased to a small value ($< V_P$), since D is at higher potⁿ & S is at lower potⁿ and there is conductive n channel in b/w having finite resistance / unit length Hence, there is a gradual potⁿ drop from D to S across the channel. With decreasing potⁿ diffⁿ across p & n along D to S, the depletion layer is also thicker most towards drain gradually decreasing in width towards source. As $V_{DS}$ is further increased, depletion layer thickens, consequently constricting the channel and thus increasing its resistance. Thus $V_{DS}$ tries to increase $I_D$ which will be decreased by increasing resistance of channel and will come to equilibrium when these opposing effects exactly cancel each other and $I_D$ does not increase though $V_{DS}$ is increased. This point is called pinch off when depletion layer physically start touching each other. $V_{DS}$ at pinch off state is called pinch off voltage.

Initially when $V_{DS} < V_P$, the transistor acts as a constant resistor (Marked by ohmic region) uptil knee pt arrives when resistance is no longer linear. from knee pt A to pinch off pt B, $I_D$ increases with $V_{DS}$ following a reverse square law.

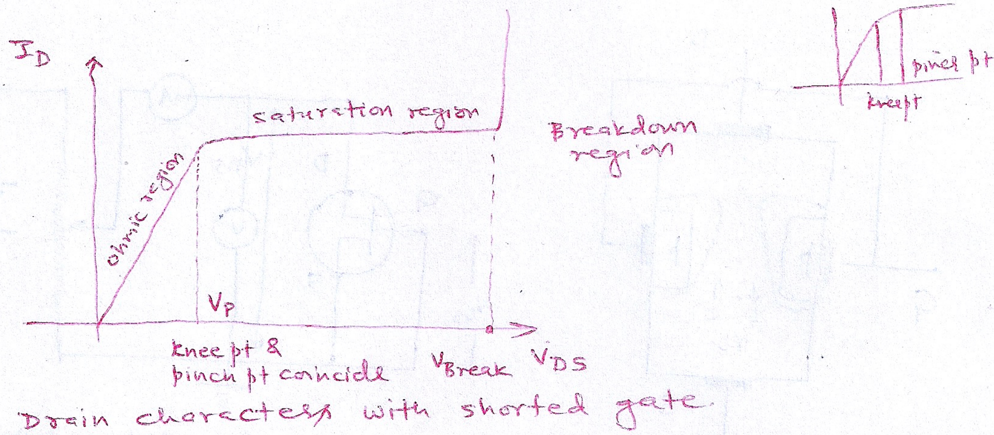
~~In region ahead~~.

CASE 3 $V_{pinch} < V_{DS} < V_{Breakdown}$.

As per Above description, $I_D$ remains const. in this region. This const value of $I_D$ at saturation is called $I_{DSS}$. However JFET cannot remain a const. current device above a certain $V_{Breakdown}$ After which Avalanche effect come into play and its conductivity increases abruptly.

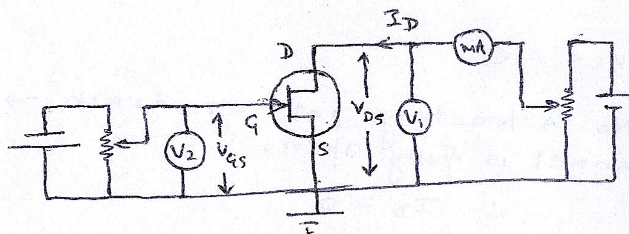
CASE 4 $V_{DS} > V_{Breakdown}$.

The channel breaks down, lot of charge carries released and current increase very rapidly and JFET may be destroyed due to heat produced in this course.




Drain characteristics with shorted gate

Drain characteristics with External Bias

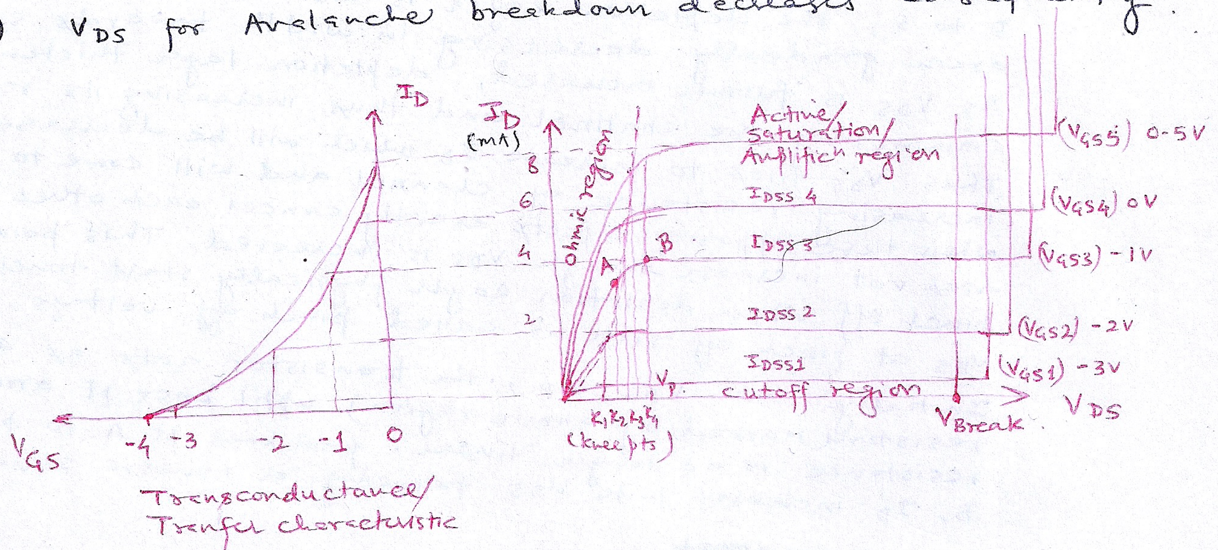



When negative gate bias voltage $V_{GS}$ is increased:

(i) saturⁿ current decreases because pinch off is achieved earlier as -ive bias supports external $V_{DS}$.

(ii) Gate channel junctions are Reversed Biased even when $V_{DS}$ is zero ie depletion region penetrates into n channel even when there is no $V_{DS}$ applied.

(iii) $V_{DS}$ for Avalanche breakdown decreases consequently.




Transconductance/ Transfer characteristic

By transfer characters it can be observed

(i) drain current decreases with the increase in negative gate-source bias.

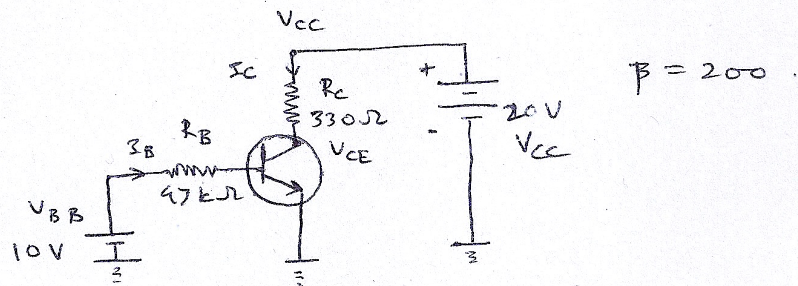
(ii) Drain current, $I_D = I_{DSS}$ when $V_{GS} = 0$.

(iii) Drain current, $I_D = 0$ when $V_{GS} = V_D$.

Advantages of BEFT over BJT

| | BJT | JEFT |
|---|---|---|
| 1. | current controlled. Biasing current is required at base terminal for operation. | voltage controlled. Biasing current not required for operation |
| 2. | BJT offer smaller input impedances, meaning they draw more current from the power circuit feeding it, which can cause loading of circuit | offer greater input impedance. Hence they draw very small current and does not load the power circuit feeding it. |
| 3. | Larger in size. Not used in ICs. | smaller & easy to fabricate. |
| 4. | | Better themal stability. |
| 5. | | Noice produced is lower. |
| 6. | | No offset voltage at zero drain current ∼ forms an excellent signal chopper. |

Q4.




$\beta = 200$.

This is a fixed bias configuration    assuming Si BJT

$$I_B = \frac{V_{BB} - V_{BE}}{R_B} = \frac{10 - 0.7}{47 \times 10^3}$$

$$\approx 0.198\ mA.$$

$$I_{CQ} = \beta I_B = 200 \times 0.198\ mA \approx \boxed{39.6\ mA}$$

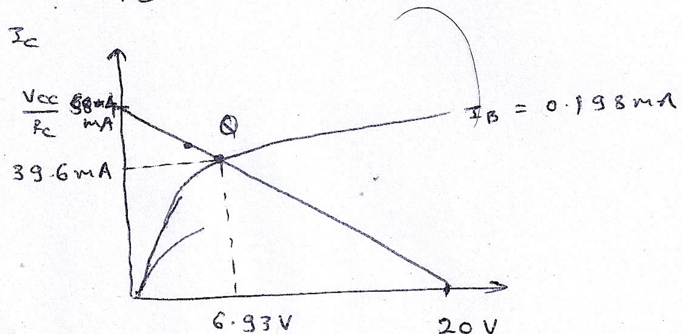
$$V_{CE} = V_{CC} - I_C R_C = 20V - 39.6mA \times 330\Omega$$

$$= 20 - 13.07V$$

$$= \boxed{6.93V}$$

~~$I_C = \frac{V_{CC} - V_{CE}}{R_C} = \frac{20 - 0.7}{330} = \frac{19.03}{330} =$~~

$$I_{cmax} = \frac{V_{CC} - V_{CE}}{R_C} = \frac{20 - 0.7}{330} = 58.4\ mA.$$




∴ Q (6.93V, 39.6mA)

— x —